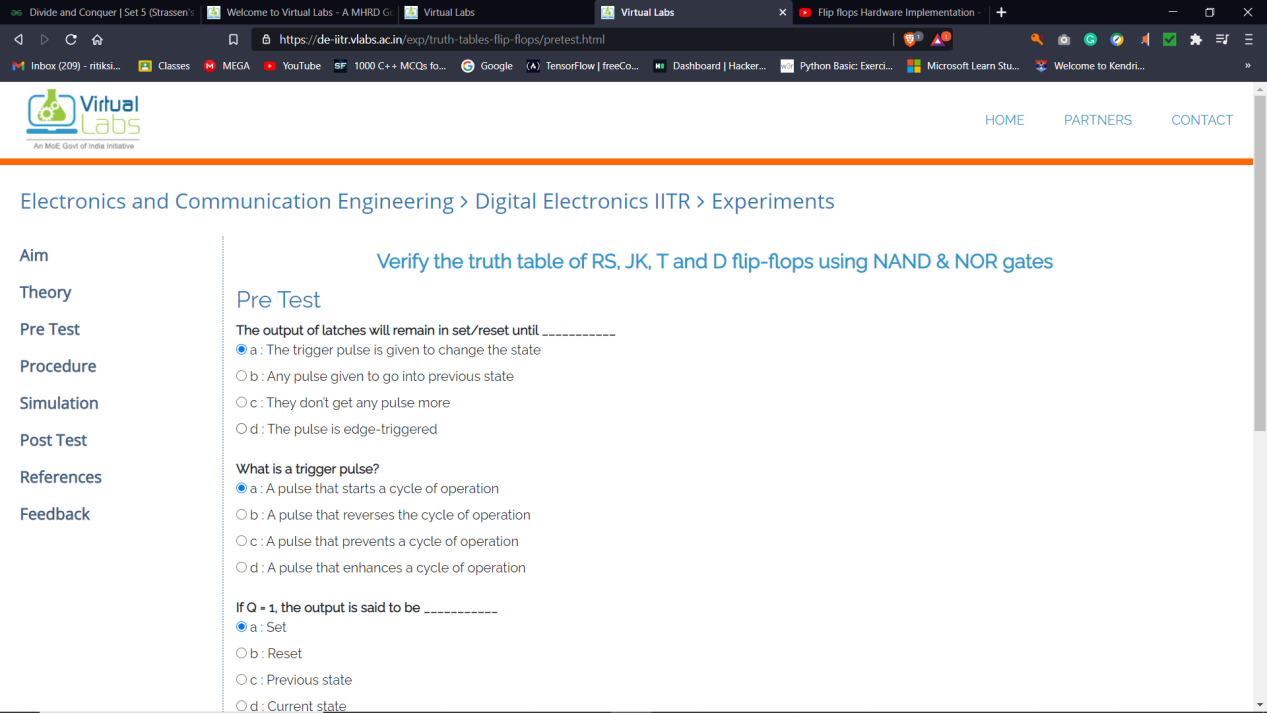
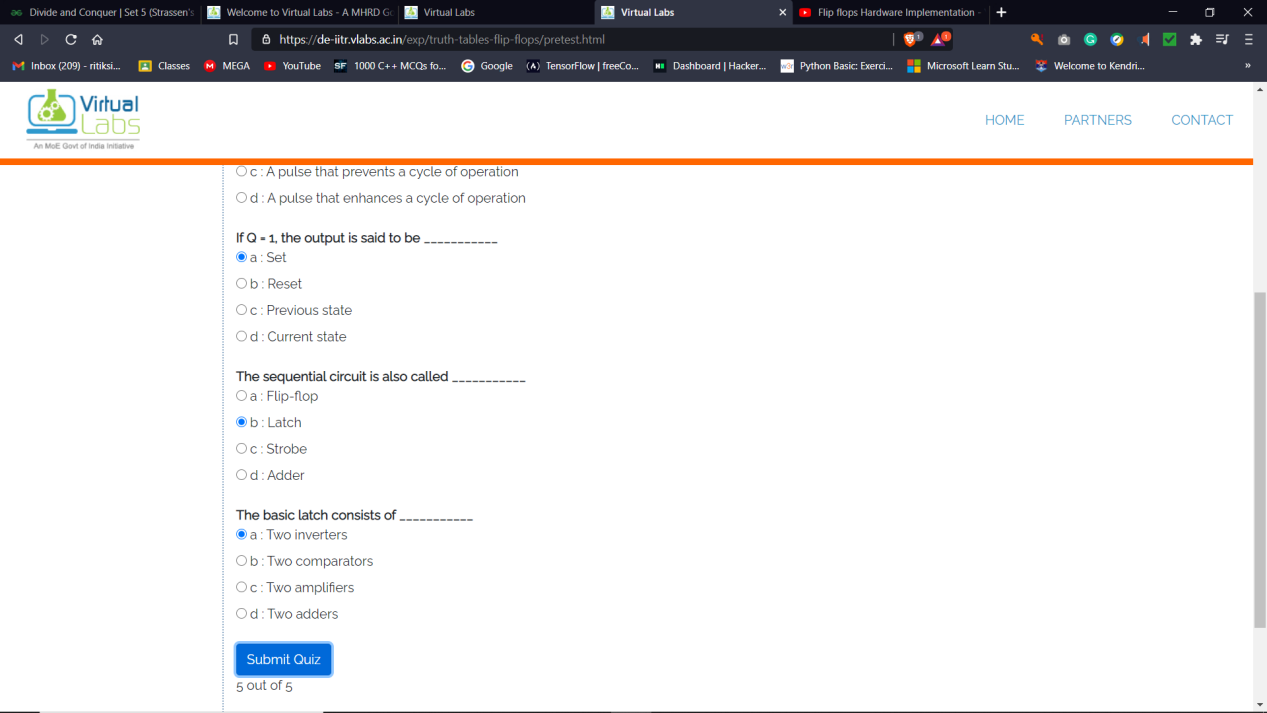
## EXPERIMENT 6

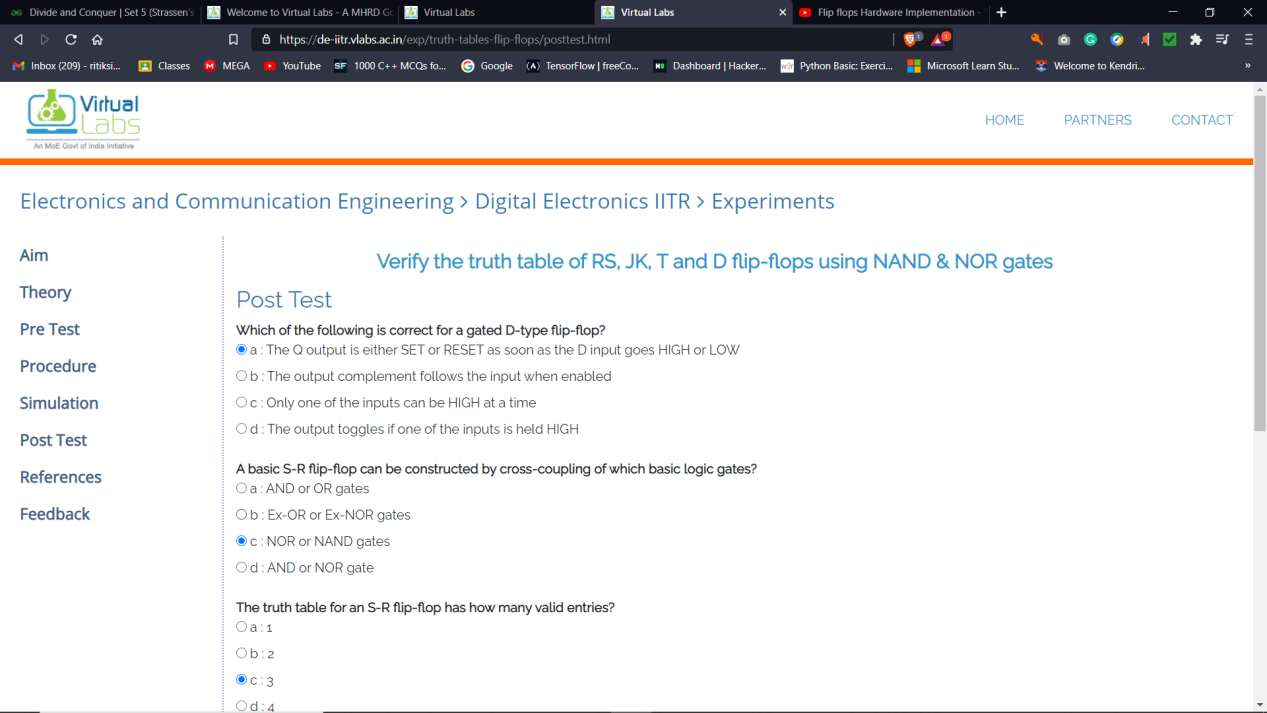
## Aim: Verify the truth table of RS, JK, T and D flip-flops using NAND & NOR gates

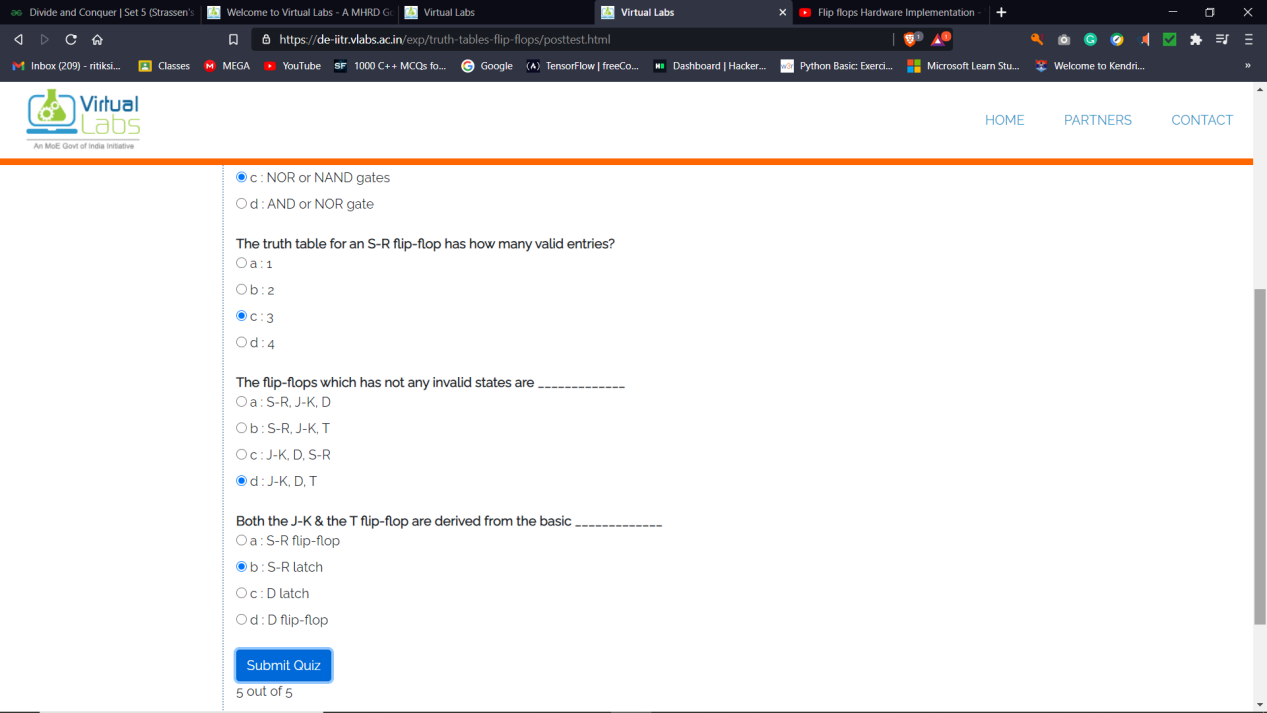
### PRE TEST





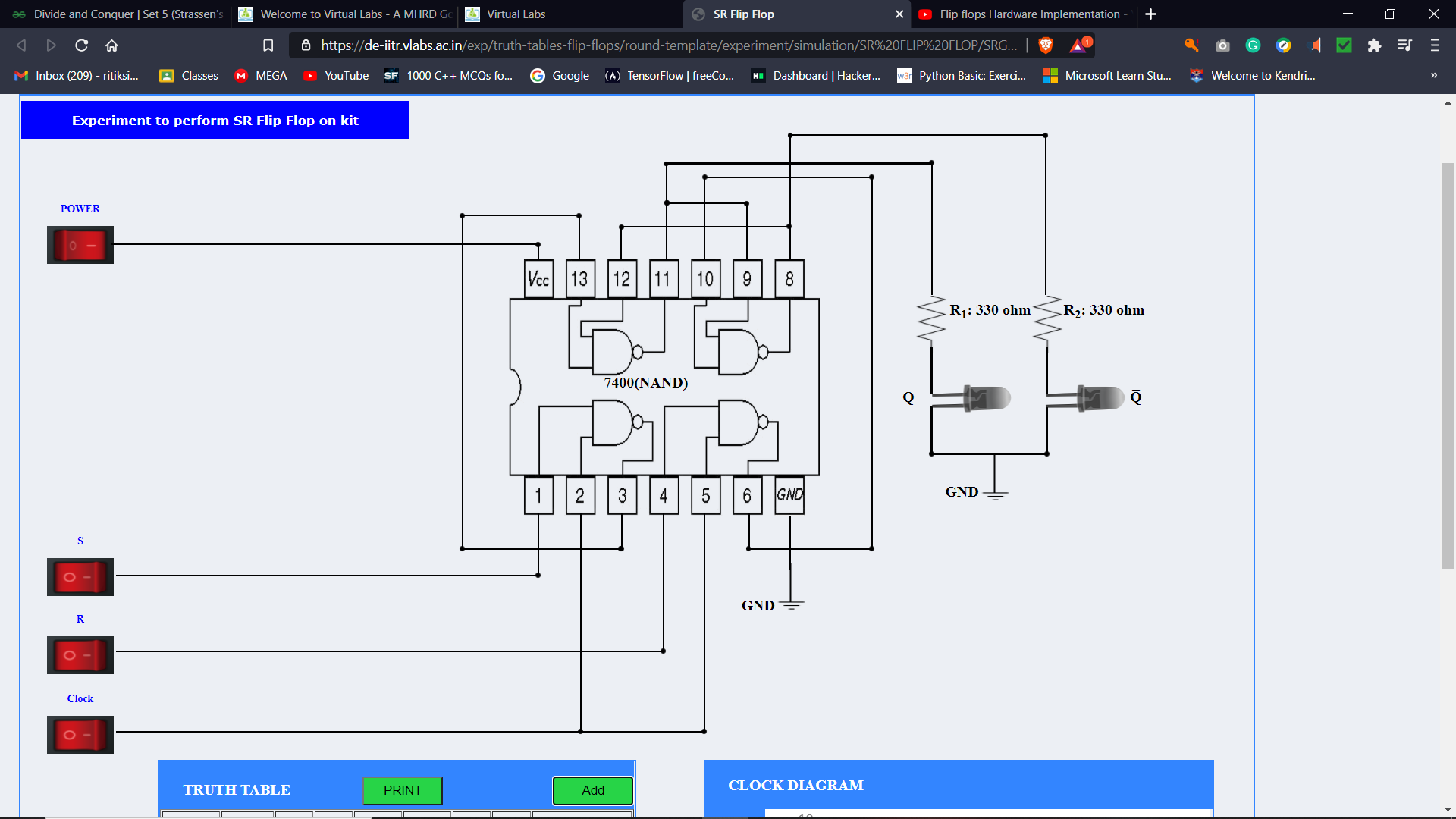
* **POST TEST**

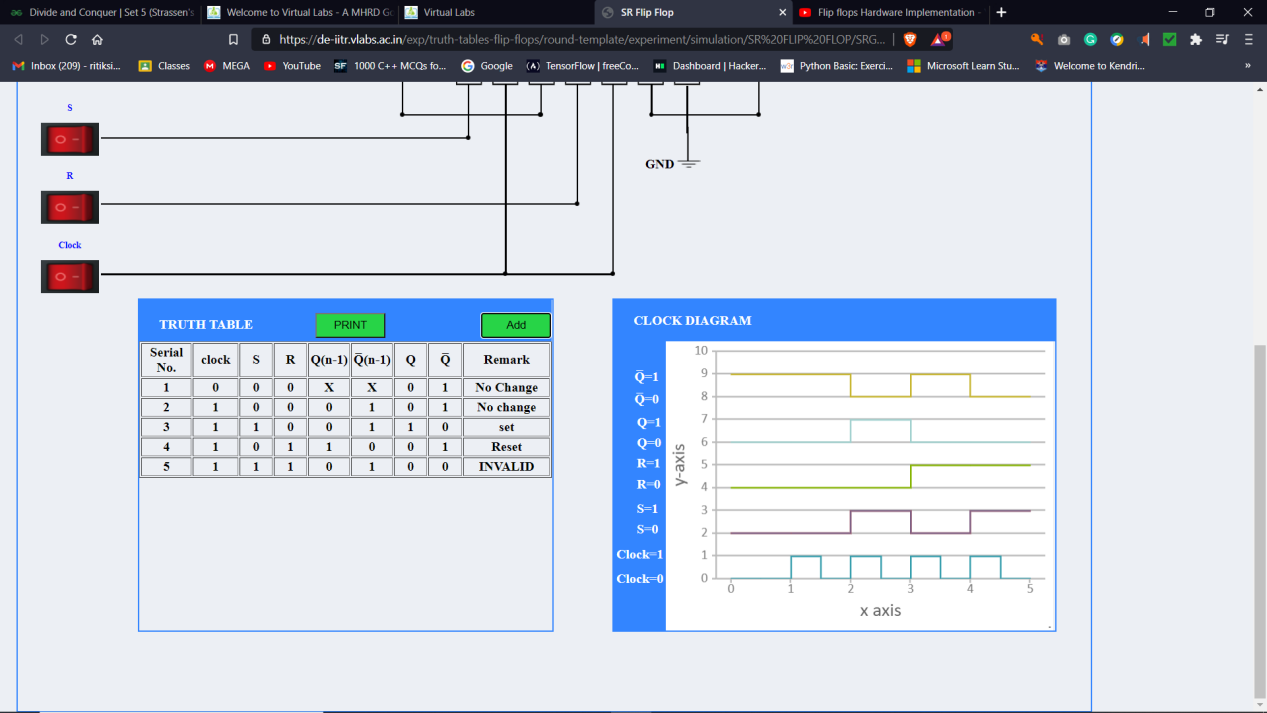
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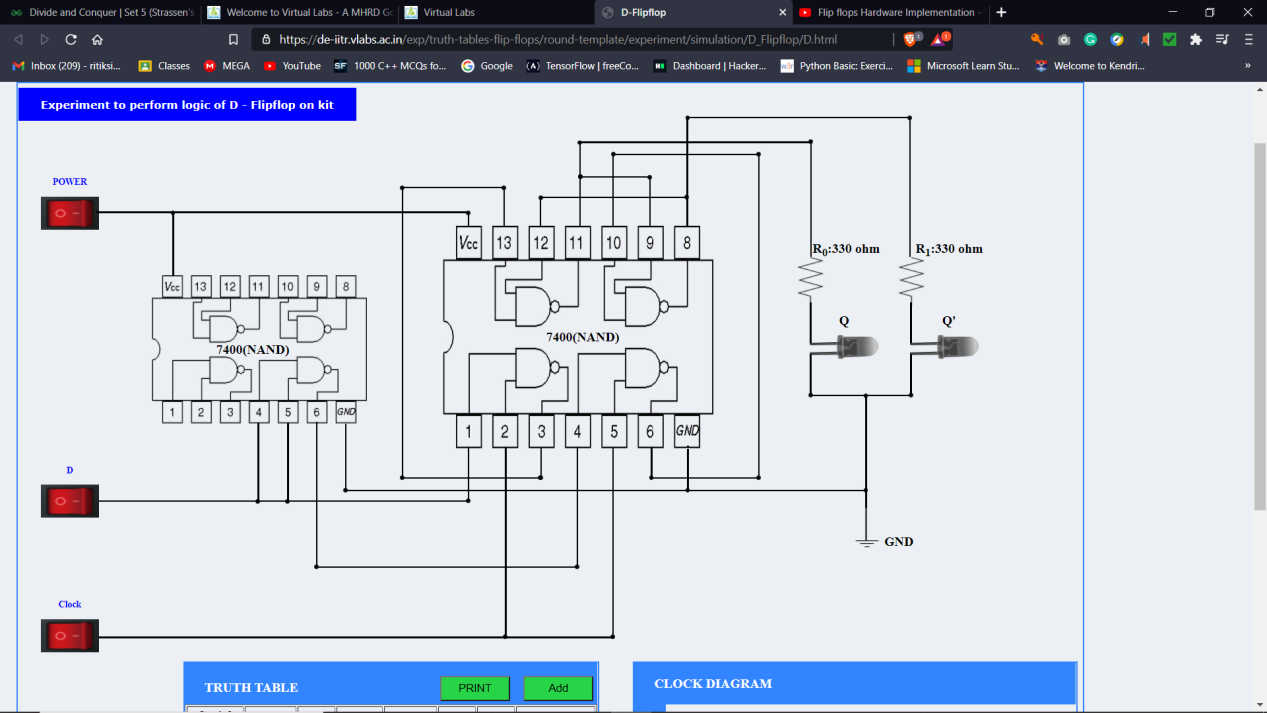
* **SIMULATION**

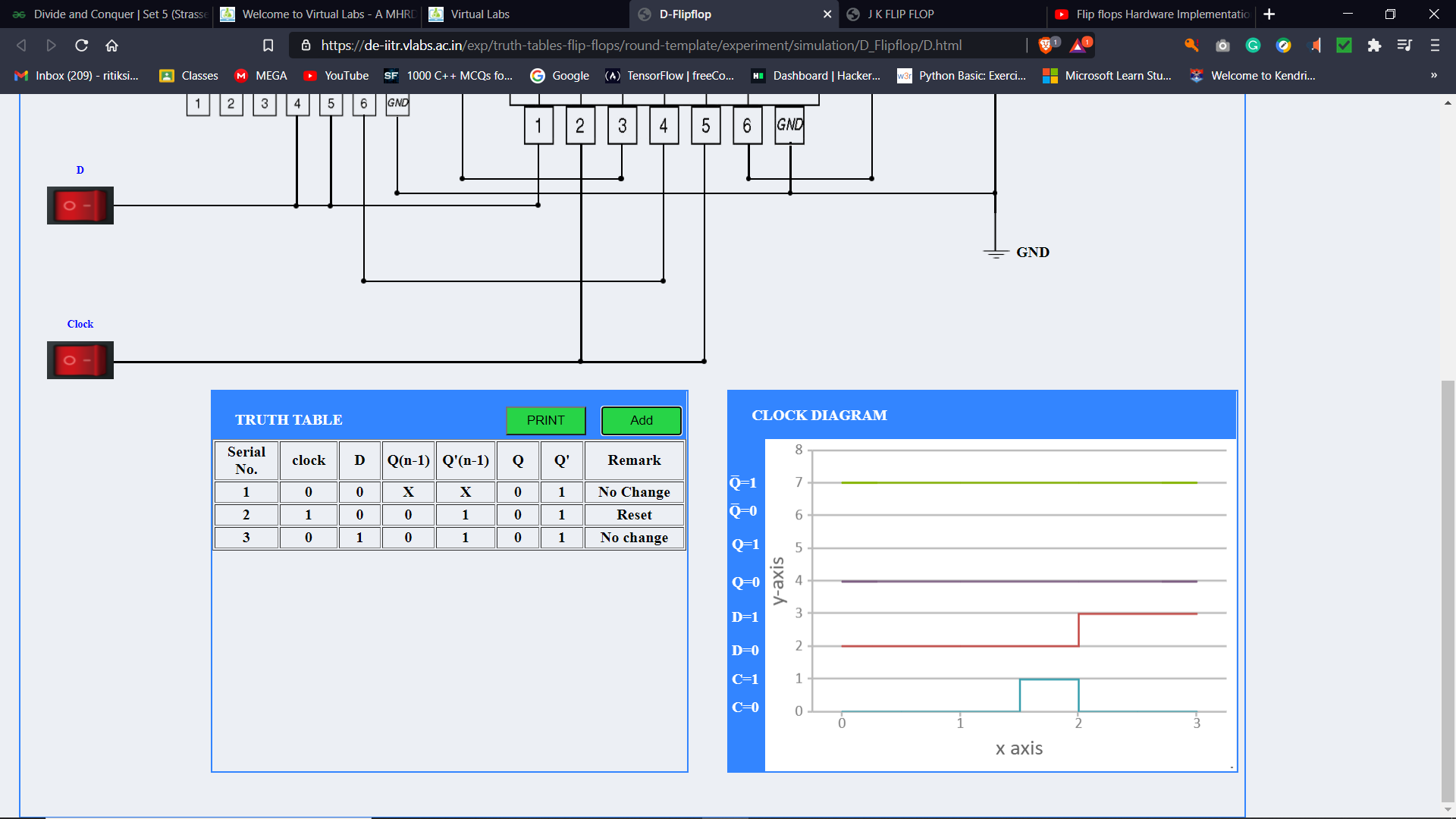
**Experiment to perform SR Flip Flop on kit**



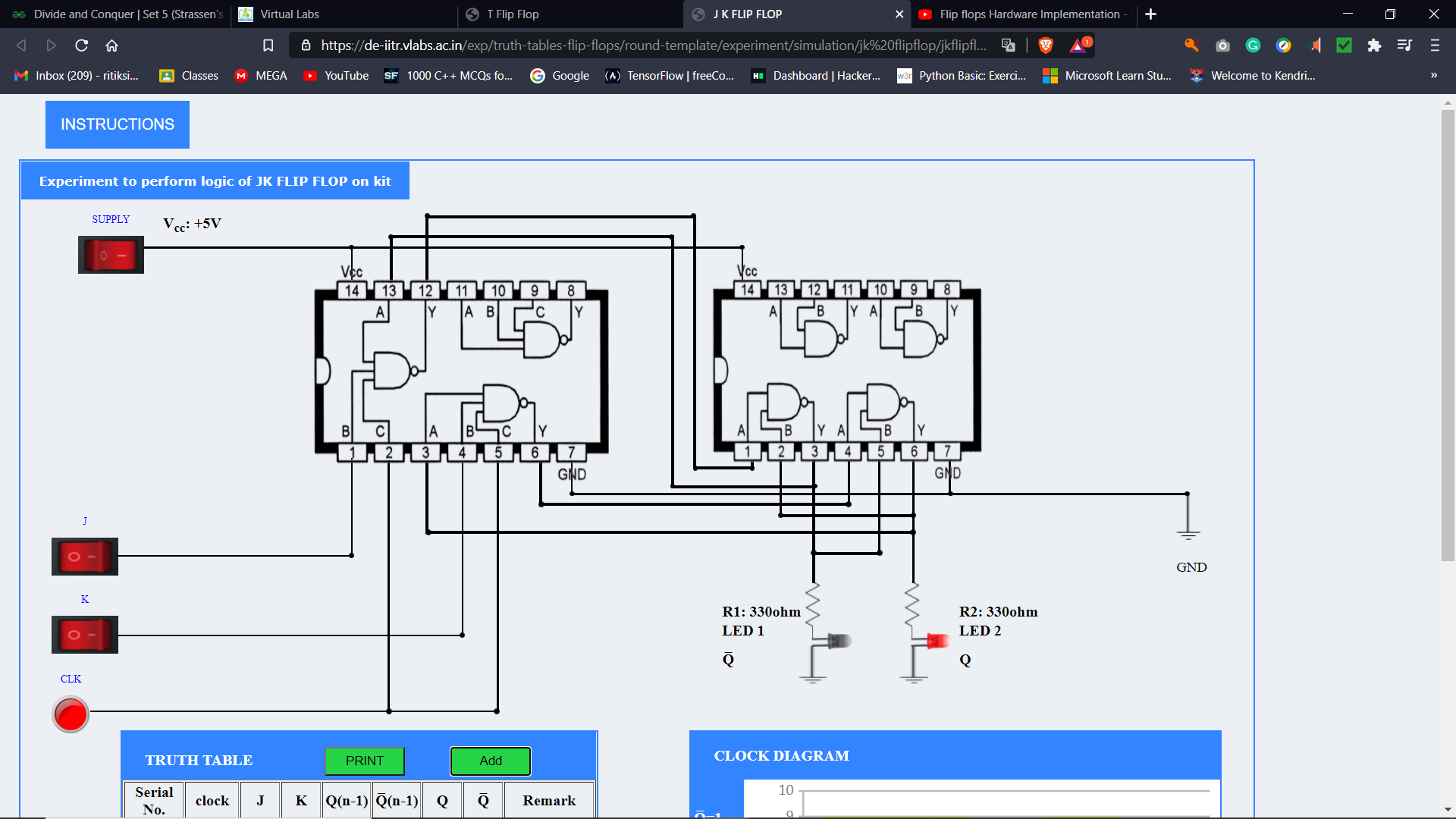


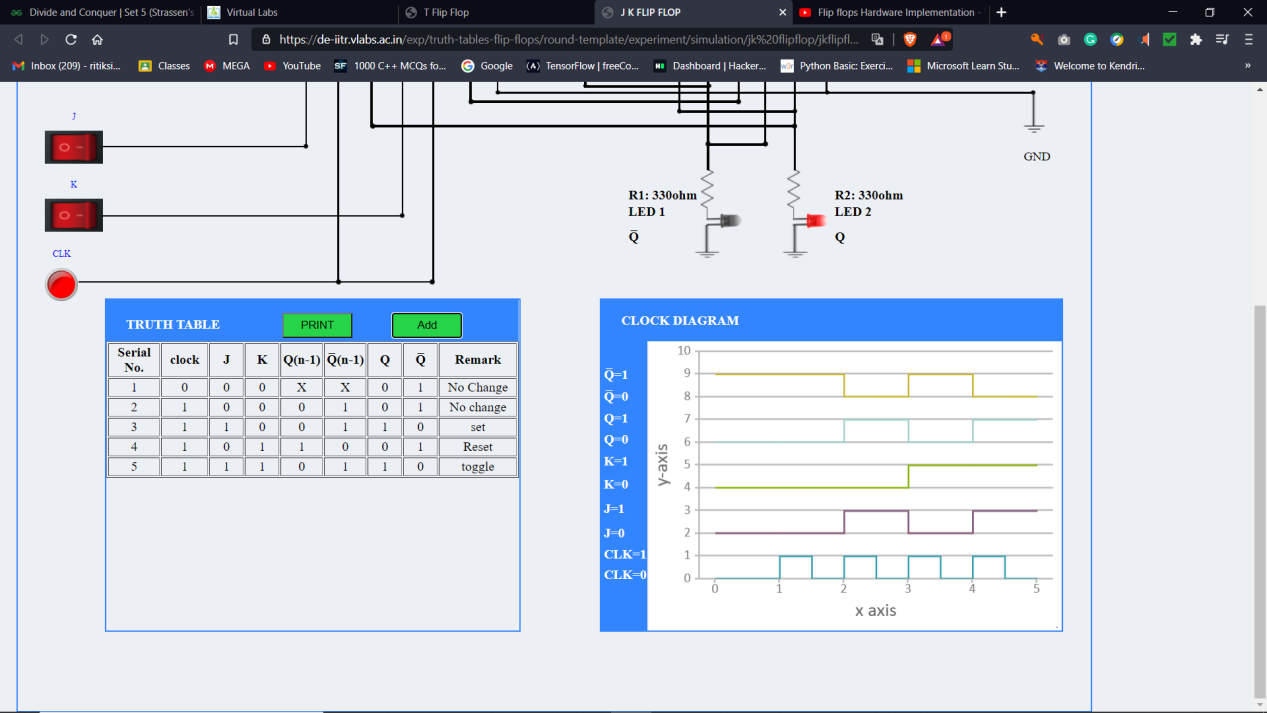
**Experiment to perform logic of D - Flipflop on kit**





**Experiment to perform logic of JK FLIP FLOP on kit**





**Experiment to perform T Flip Flop on kit**

